盛微先進科技
SAVITECH.COM

BRAVO
SA9123

Stereo In/Out
PCM 24Bit/192KHz
USB Audio Streaming Controller

Datasheet v1.0

SAVITECH Corporation

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BRAVO-PCM
SA9123
USB Audio Streaming Controller

Overview

The SA9123 is a high performance up to 24bit, 192KHz PCM streaming USB High-Speed compliant audio steaming controller. It features one stereo playback and recording pairs. The SA9123 is ideal for both one stereo-in and one stereo-out professional digital audio interface applications. Its PCM resolution and playback sampling rate can be configurable with 16/24 bit and 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192KHz respectively.

Features

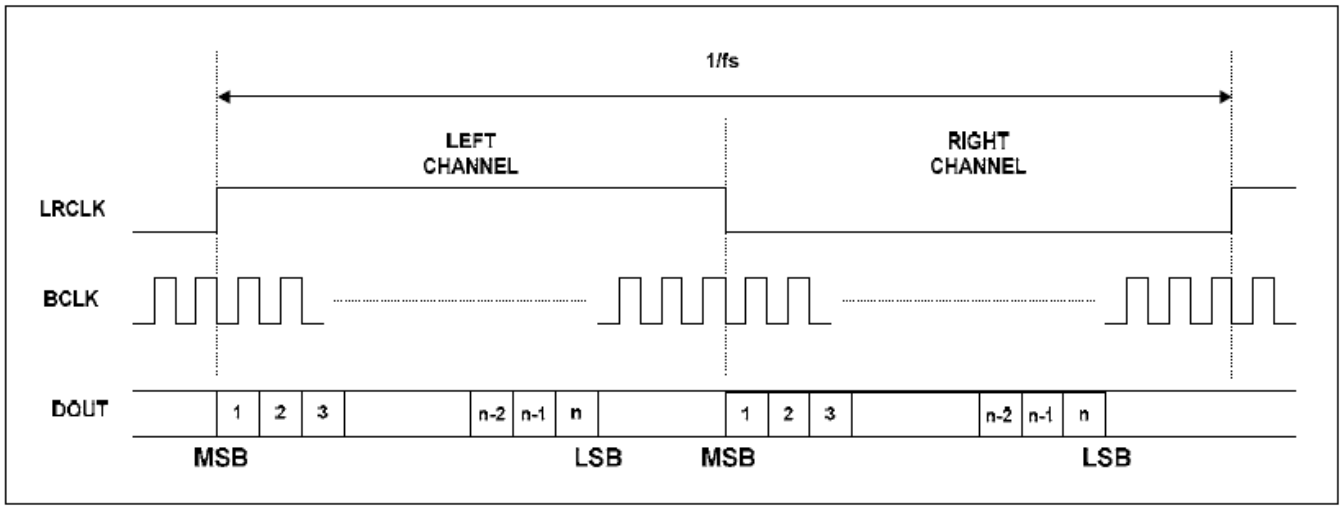
- SA9123 optional iAP1/iAP2, require MFi (Made for iDevice) license
- USB 2.0 High-Speed Compliant
- USB Audio Class v1.0 and v2.0 supported
- Incredible Bravo sound quality supported by Savitech innovative Bravo Tech
  - Bravo Tech*1 supporting Jitter-less outputs using local clock in Async-mode
- Isochronous input and output endpoints for recording and playback
- One interrupt endpoint for HID
- Support resolutions up to 24-bit and sampling rates up to 192KHz
- Two I2S input pairs and two I2S output pairs for PCM
  - Independent sample rates for each pairs
  - 32/ 44.1/ 48/ 88.2/ 96/ 176.4/ 192KHz playback sampling rates
  - 44.1/ 48KHz record sampling rates
  - 16/24bit resolution
- Control and I/O
  - I2C bus
  - GPIOs
- 64-pin TQFP packages

For iDevice, it is necessary to become a licensee of Apple Inc.

Serial Audio Interfaces Formats

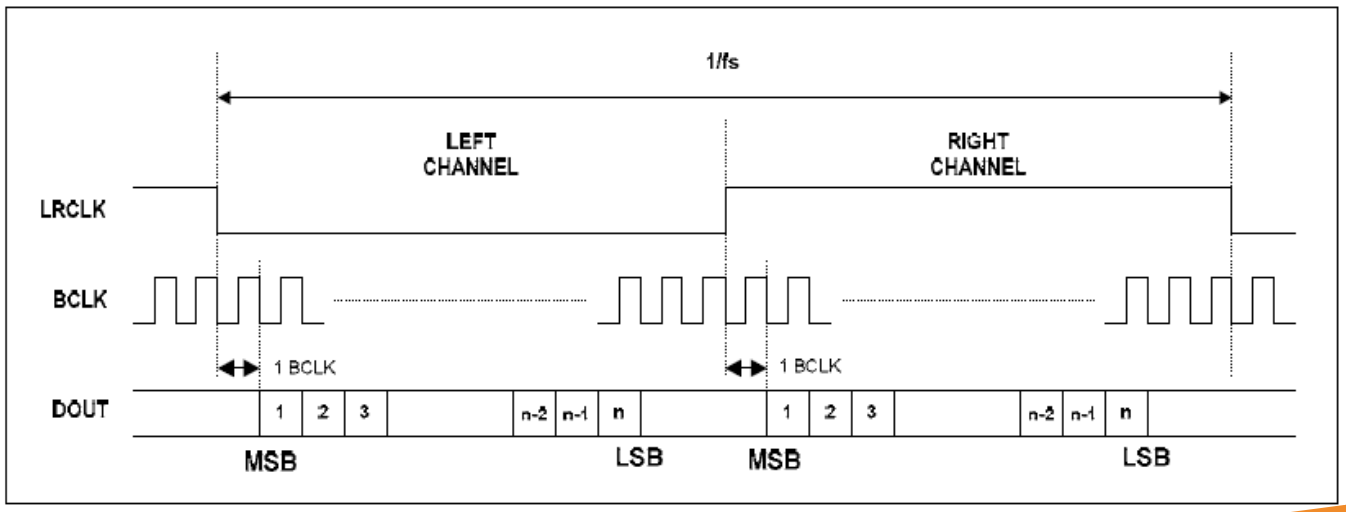
■ L-justified format:

In Left Justified mode, the MSB is available on the first rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.



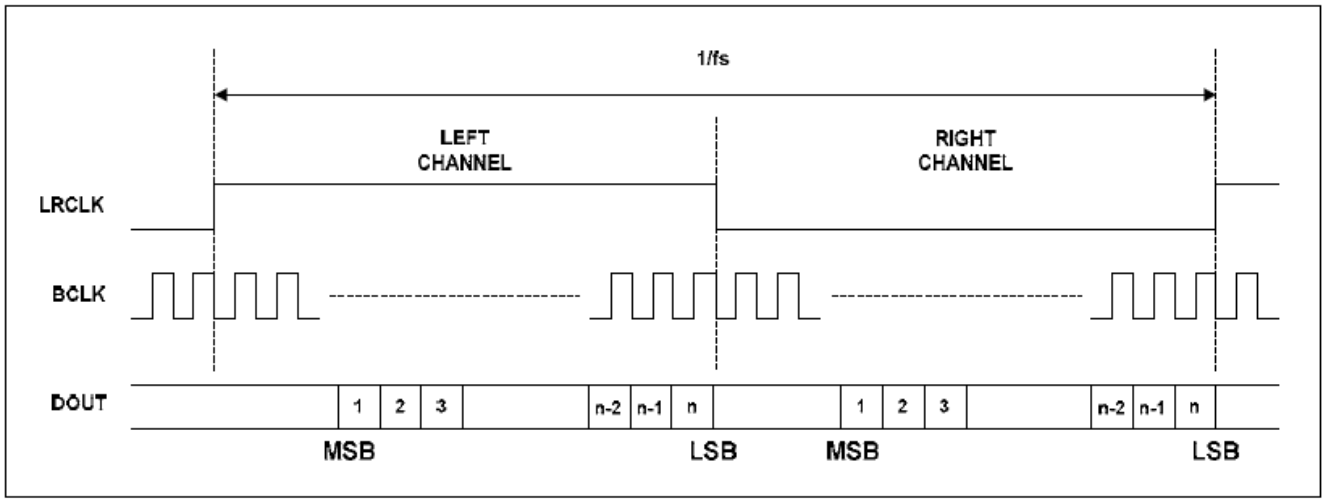
■ I2S format

In I2S mode, the MSB is available on the second rising edge of BCLK following an LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.



■ R-justified format

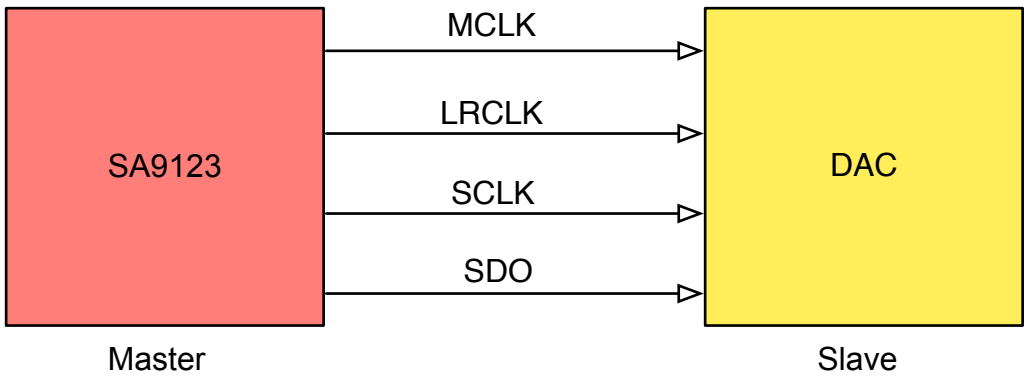
In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition. In Right Justified mode, the LSB is available on the last rising edge of BCLK before an LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.



Serial Audio Interfaces Configuration-DAC

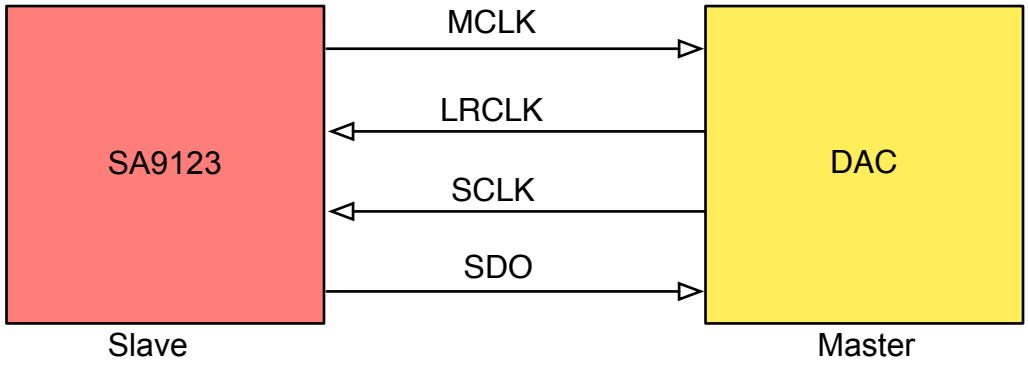
■ SA9123 supports both master mode and slave mode for following configurations.

■ **Master Mode**



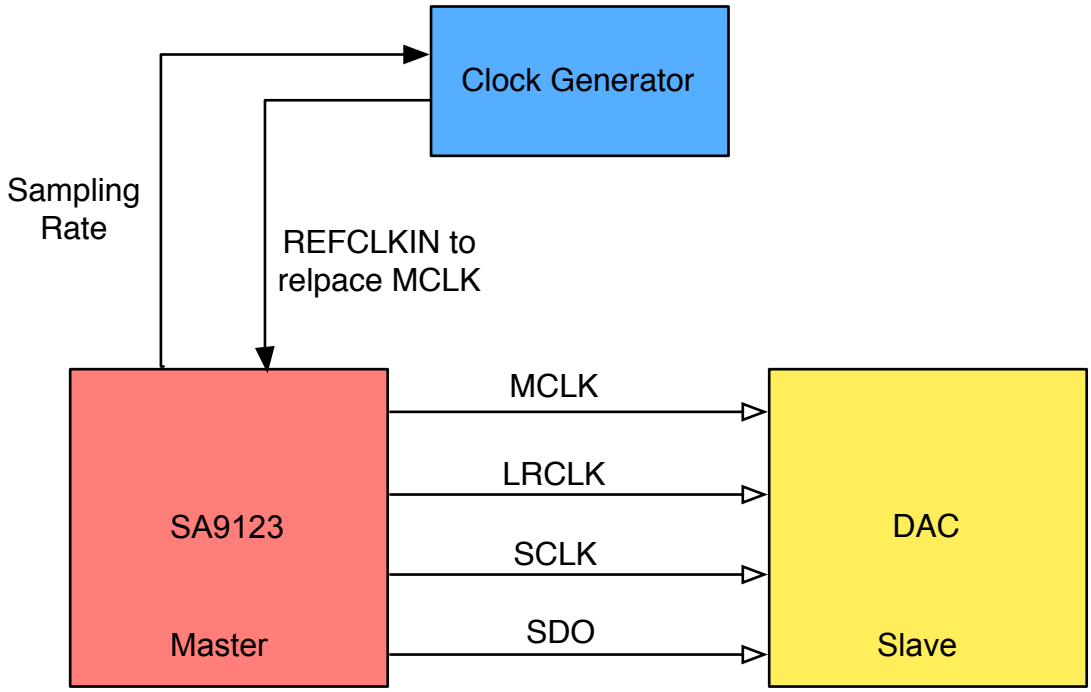
SA9123 I2S Master Mode connection

■ **Slave Mode**

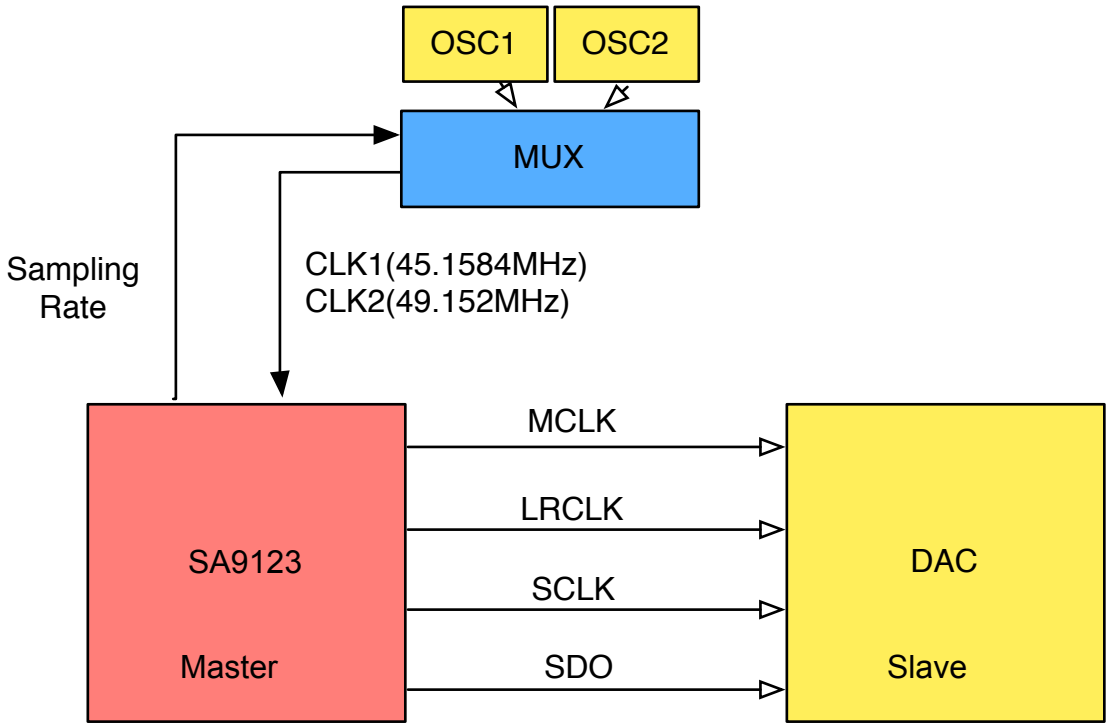


SA9123 I2S Slave Mode connection

Serial Audio Interfaces Configuration-DAC

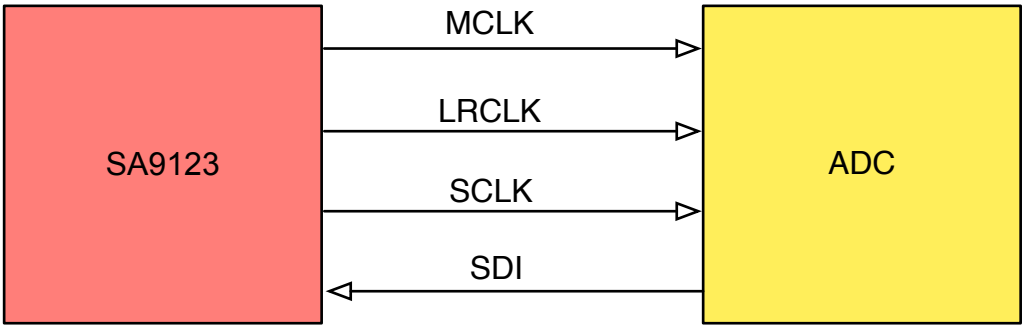


Master Mode (with external REFCLKIN), Mode 0



Master Mode (with external REFCLKIN), Mode 1

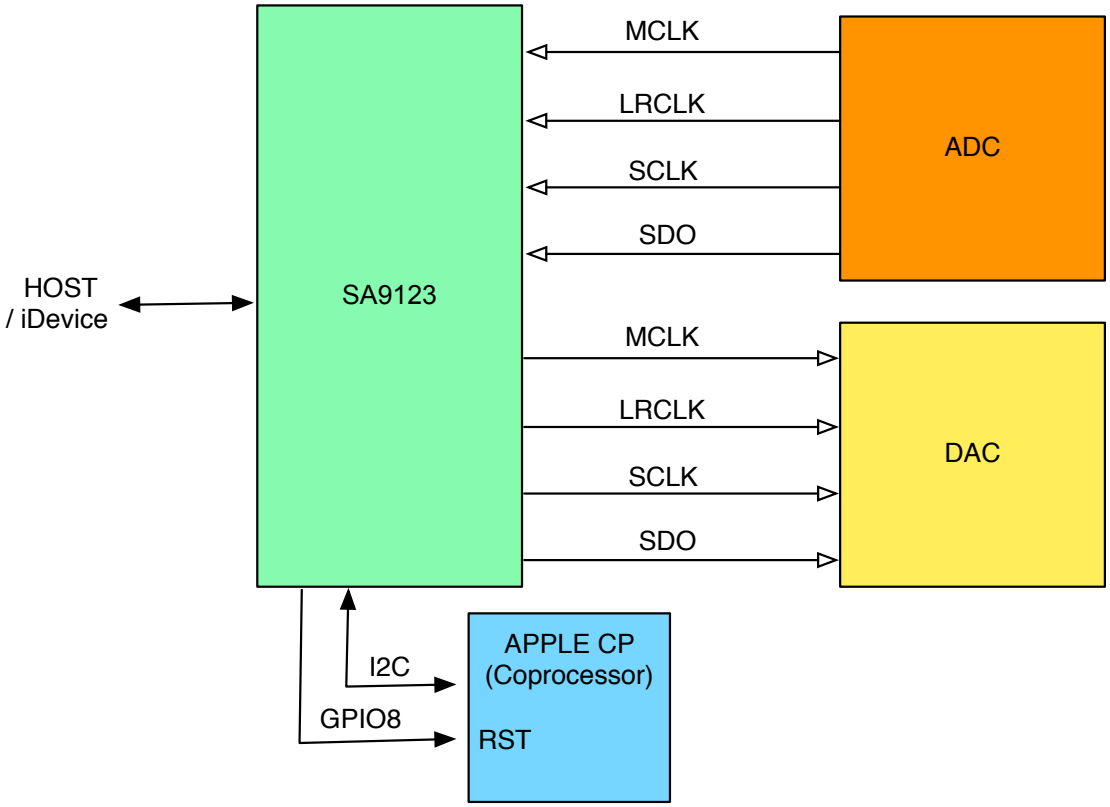
Serial Audio Interfaces Configuration-ADC



iDevice support

Apple strongly recommends the use of digital audio paths to and from accessories. Apple device in USB Host Mode audio is the recommended approach. SA9123 will authenticate and identify itself to Apple device using iAP1/iAP2 CP before the iDevice will enumerate and start using USB Audio interface.

- Support 16 /24-bit linear PCM
- Support 44.1, 48KHz sampling rate and up to 192KHz.
- Support input and output audio interface
- Support Volume Control Feature Unit
- Support iAP1 and iAP2 by CP2.0B and CP2.0C.



Digital USB Audio Application for iDevice

For using of SA9123 on iDevice, It is necessary to become a licensee of Apple Inc. regarding "Made for iPod/iPhone/iPad License".

I²C Master Interfaces

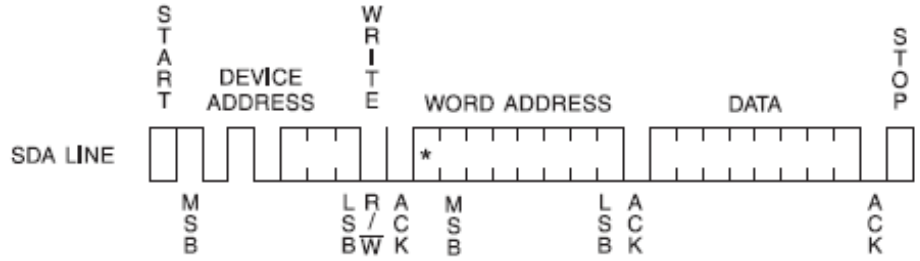
One serial I²C master is supported in SA9123 to control external peripheral devices (EEPROM). SA9123 need an EEPROM to load Firmware code from it.
SA9123 support use I²C Master Interfaces to read/write CP to support Apple MFi.

I²C Slave Interfaces

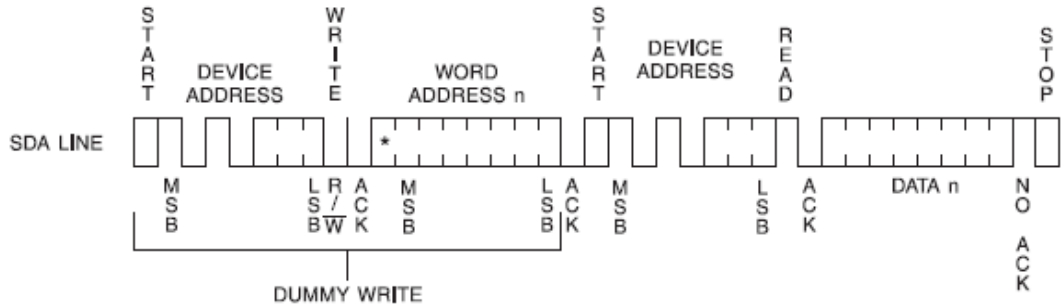
SA9123 have an I2C slave interface which is used for external uC to read status of SA9123.

I2C supports burst read /burst write.

Byte Write



Random Read



Pin Assignment

Pin	Name	Pin	Name
1	VDD33_LDO	33	GPIO4
2	GND_LDO	34	GPIO5
3	LDO18OUT	35	GPIO6
4	VDD	36	GPIO7
5	GND	37	GPIO8
6	NC	38	RESETN
7	VDD	39	VDD
8	VDD18	40	SCL_M
9	SOF_FLAG	41	SDA_M
10	NC	42	DSCLK
11	NC	43	VDD18
12	REXT	44	VDD
13	VDD	45	DDATA
14	VDD	46	DMCLK
15	DP	47	DLRCK
16	DM	48	NC
17	GND	49	ASCLK
18	XI	50	ADATA
19	XO	51	AMCLK
20	VDD18	52	VDD
21	VDD	53	ALRCK
22	GND	54	SCL_S
23	GND	55	SDA_S
24	VDD	56	VDD
25	GND	57	REFCLKIN
26	VDD	58	VDD18
27	GPIO0	59	TEST1
28	VDD18	60	TEST2
29	VDD	61	TEST3
30	GPIO1	62	TEST4
31	GPIO2	63	TEST5
32	GPIO3	64	TEST6

Pin Description

Pin	Name	I/O/P	Description
1	VDD33_LDO	P	LDO Input
2	GND_LDO	P	LDO Ground
3	LDO18_OUT	P	LDO Output
4	VDD	P	I/O power
5	GND	P	I/O ground
6	NC	-	NC
7	VDD	P	I/O power
8	VDD18	P	Core power
9	SOF_FLAG	O	USB SOF(Start Of Frame) indicator
10	NC	-	NC
11	NC	-	NC
12	REXT	I	Connect 270ohm resistor to ground
13	VDD	P	USB2.0 PHY power
14	VDD	P	USB2.0 PHY power
15	DP	I/O	USB2.0 signals
16	DM	I/O	USB2.0 signals
17	GND	P	USB2.0 PHY ground
18	XI	I/O	12MHz X'stal
19	XO	I/O	12MHz X'stal
20	VDD18	P	USB2.0 PHY power
21	VDD	P	PLL power
22	GND	P	PLL ground
23	GND	P	PLL ground
24	VDD	P	PLL power
25	GND	P	PLL ground
26	VDD	P	PLL power
27	GPIO0	I/O	General purpose I/O
28	VDD18	P	Core power
29	VDD	P	I/O power
30	GPIO1	I/O	General purpose I/O
31	GPIO2	I/O	General purpose I/O
32	GPIO3	I/O	General purpose I/O

Pin	Name	I/O/P	Description
33	GPIO4	I/O	General purpose I/O
34	GPIO5	I/O	General purpose I/O
35	GPIO6	I/O	General purpose I/O
36	GPIO7	I/O	General purpose I/O
37	GPIO8	I/O	For Apple CP reset
38	RESETN	I	Power-on reset signal (active low)
39	VDD	P	I/O power
40	SCL_M	I/O	Master I2C clock
41	SDA_M	I/O	Master I2C data
42	DSCLK	I/O	I2S output SCLK
43	VDD18	P	Core power
44	VDD	P	I/O power
45	DDATA	O	I2S output data
46	DMCLK	I/O	I2S output MCLK
47	DLRCK	I/O	I2S output LRCLK
48	NC	O	NC
49	ASCLK	I/O	I2S input SCLK
50	ADATA	I	I2S input data pin
51	AMCLK	I/O	I2S input MCLK
52	VDD	P	I/O power
53	ALRCK	I/O	I2S input LRCLK
54	SCL_S	I/O	Slave I2C CLK
55	SDA_S	I/O	Slave I2C SDA
56	VDD	P	I/O power
57	REFCLKIN	I	Optional external reference clock input
58	VDD18	P	Core power
59	TEST1	I	Normal Operation need pull-high
60	TEST2	I	Normal Operation need pull-down
61	TEST3	I	Normal Operation need pull-down
62	TEST4	I	Normal Operation need pull-down
63	TEST5	I	Normal Operation need pull-down
64	TEST6	I	Normal Operation need pull-down

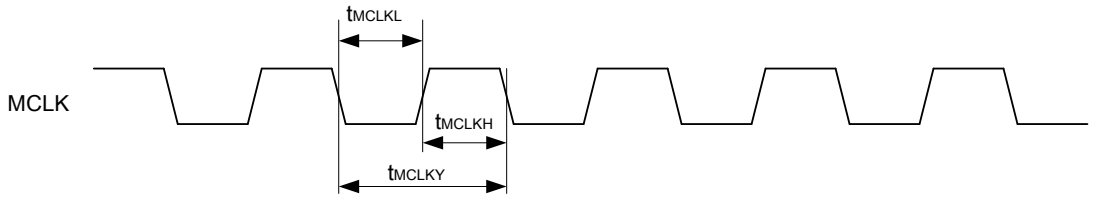
DC Characteristics

Test Conditions: Ta = 25°C; VDD33 = +3.0 ~ +3.6V; fs = 48 kHz-32bit sine wave

Parameter	Symbol	Test Condition	Min.	Max.	Unit
Input Low Voltage	VIL	VD33 = 3.3V		0.3*VDD33	V
Input High Voltage	VIH	VDD33 = 3.3V	0.7*VDD33		V
Output Low Voltage	VOL	IOL = 2mA		0.2	V
Output High Voltage	VOH	IOH = -2mA	VDD33-0.2		V
Input Low Leakage Current	IIL	VIN = 0V VDD33 = 3.6V	-10	10	uA
Input High Leakage Current	IIH	VIN = 3.6V VDD33 = 3.6V	-10	10	uA
Operation Power Current		VDD33 = 3.3V VDD18 = Ext. DC-DC Normal Mode		72	mA
Operation Power Current		VDD33 = 3.3V VDD18 = Ext. DC-DC Low Power Mode		52	mA

AC Timing Characteristics

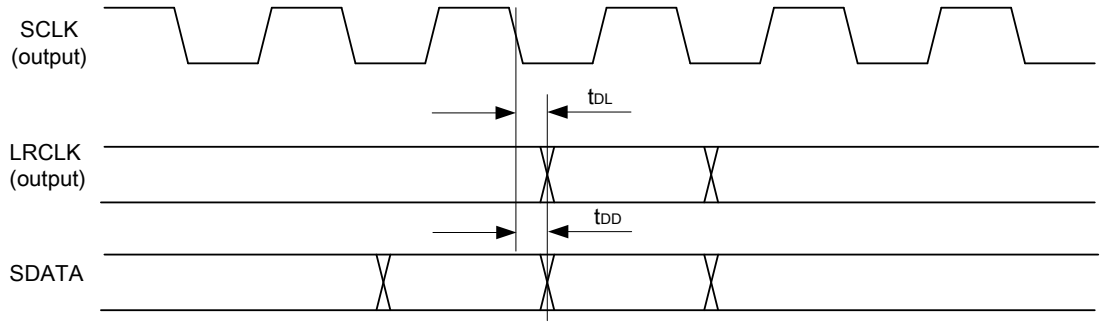
1. System Clock Timing



Test Conditions: VDD = 3.3V, VSS = 0V, TA = +25°C, Master Mode fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
MCLK System clock pulse width high	tMCLKL		41.13		ns
MCLK System clock pulse width low	tMCLKH		40.23		ns
MCLK System clock cycle time	tMCLKY		81.36		ns

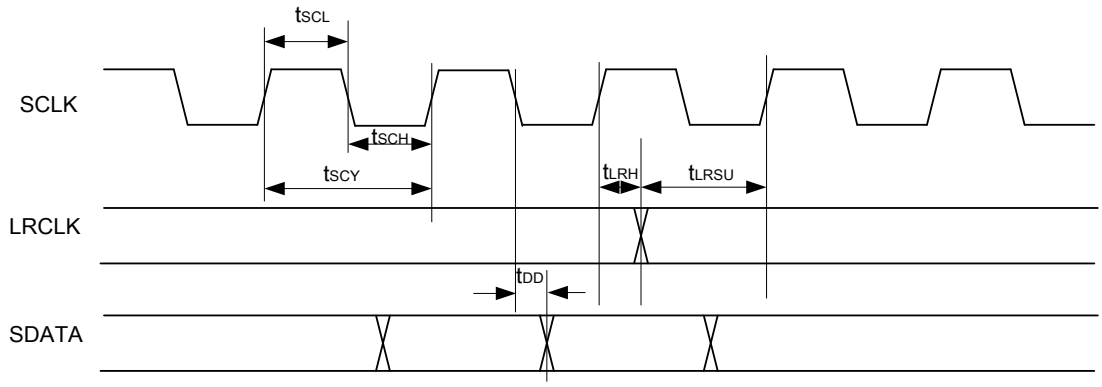
2. Audio Interface Timing – Master Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
LRCLK propagation delay from SCLK falling edge	tDL	5			ns
SDATA propagation delay from SCLK falling edge	tDDA	5			ns

3. Audio Interface Timing – Slave Mode



Test Conditions: VDD = V, VSS = 0V, TA = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data.

Parameter	Symbol	Min	Typ.	Max	Unit
SCLK cycle time	tSCY	293	325	358	ns
LRCLK pulse width high	tSCH	144	163	179	ns
SCLK pulse width low	tSCL	144	163	179	ns

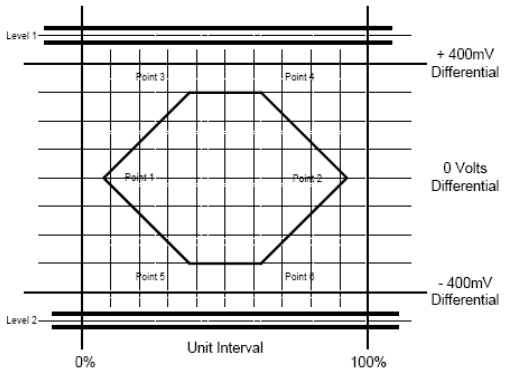
LRCLK set-up time to SCLK rising edge	tLRSU	10			ns
LRCLK hold time from SCLK rising edge	tLRH	10			ns
SDATA propagation delay from SCLK falling edge	tDD	5			ns

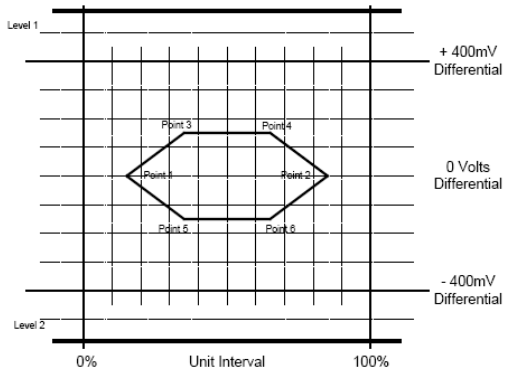
Dynamic Electrical Characteristics: (DP/DM)

Driver Characteristics:

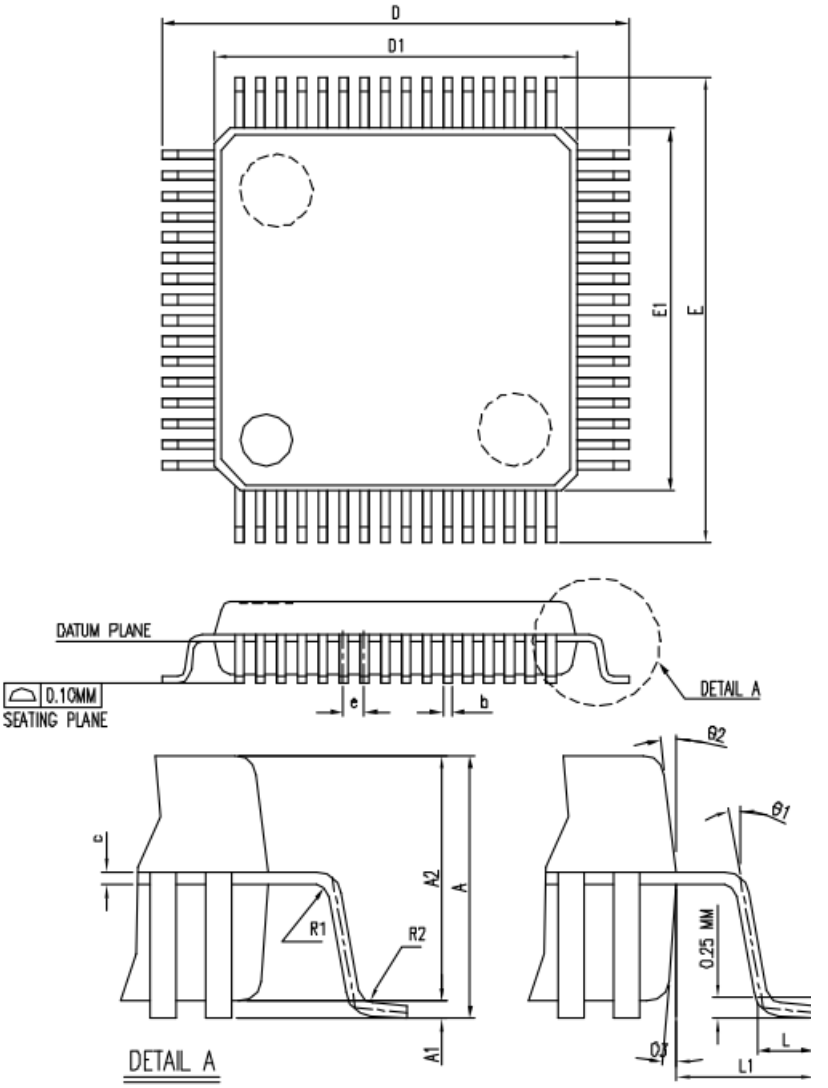
Symbol	Parameter	Min	Max	Unit
High-speed Mode				
t_{HSR}	High-speed differential rise time (10% - 90%)	500	-	ps
t_{HSF}	High-speed differential fall time (10% - 90%)	500	-	ps
Full-speed Mode				
t_{FR}	Rise Time for DP/DM	4	20	ns
t_{FF}	Fall Time for DP/DM	4	20	ns
t_{FRFM}	Differential rise/fall Time Matching (t_{FR} / t_{FF})	90	110	%
V_{CRS}	Output Signal Crossover Voltage	1.3	2.0	V

Driver Timing/Receiver timing:

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver timing						
High-speed mode						
Driver waveform requirement	See the eye pattern of template 1 (described in the USB 2.0 spec.) 	Follow template 1 described in USB specification Rev 2.0. <table><tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr><tr><td>Level 1</td><td>525 mV in UI following a transition, 475 mV in all others</td><td>N/A</td></tr><tr><td>Level 2</td><td>-525 mV in UI following a transition, -475 in all others</td><td>N/A</td></tr><tr><td>Point 1</td><td>0 V</td><td>7.5% UI</td></tr><tr><td>Point 2</td><td>0 V</td><td>92.5% UI</td></tr><tr><td>Point 3</td><td>300 mV</td><td>37.5% UI</td></tr><tr><td>Point 4</td><td>300 mV</td><td>62.5% UI</td></tr><tr><td>Point 5</td><td>-300 mV</td><td>37.5% UI</td></tr><tr><td>Point 6</td><td>-300 mV</td><td>62.5% UI</td></tr></table>			
Full-speed mode						

<table>
<tr><td>Propagation delay
(VI, FSE 0, OE to
DP, DM)</td><td colspan="2">For the detailed description of VI, FSE 0, and OE, (please refer to the USB 1.1 spec.)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
<tr><td colspan="7">Receiver timing</td></tr>
<tr><td colspan="7">High-speed mode (template 4, USB 2.0 spec.)</td></tr>
<tr><td>Data source jitter and receiver jitter tolerance</td><td colspan="2">See the eye pattern of template 4 (described in the USB 2.0 spec.)
 
</td><td colspan="4">Follow template 4 described in USB specification Rev 2.0.
<table><tr><th></th><th>Voltage Level (D+ - D-)</th><th>Time (% of Unit Interval)</th></tr><tr><td>Level 1</td><td>575 mV</td><td>N/A</td></tr><tr><td>Level 2</td><td>-575 mV</td><td>N/A</td></tr><tr><td>Point 1</td><td>0 V</td><td>15% UI</td></tr><tr><td>Point 2</td><td>0 V</td><td>85% UI</td></tr><tr><td>Point 3</td><td>150 mV</td><td>35% UI</td></tr><tr><td>Point 4</td><td>150 mV</td><td>65% UI</td></tr><tr><td>Point 5</td><td>-150 mV</td><td>35% UI</td></tr><tr><td>Point 6</td><td>-150 mV</td><td>65% UI</td></tr></table></td></tr>
<tr><td colspan="7">Full-speed mode</td></tr>
<tr><td>$t_{PLH(rcv)}$
$t_{PHL(rcv)}$</td><td>Receiver propagation delay (DP; DM to RX_RCV)</td><td>For the detailed description of RCV, (please refer to the USB 1.1 spec.)</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
<tr><td>$t_{PLH(single)}$
$t_{PHL(single)}$</td><td>Receiver propagation delay (DP; DM to VOP, VON)</td><td>-</td><td>-</td><td>-</td><td>15</td><td>ns</td></tr>
</table>

TQFP 64 MECHANICAL DATA



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.0019		0.0059
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09		0.20	0.0035		0.0078
e	0.40 BASIC			0.016 BASIC		
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.0031		
R2	0.08		0.20	0.0031		0.0078
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
JEDEC	MS-026 (BBD)					

*NOTES : DIMENSIONS " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.